ABSTRACT OF THE DISCLOSURE

A semiconductor device constructed by mounting a plurality of chip intellectual properties (IPs) on a common semiconductor wiring substrate, a method for testing the device and a method for mounting the chip IPs. A silicon wiring substrate on which chip IPs can be mounted is provided. A circuit for a boundary scan test is formed on the silicon wiring substrate by connecting flip flops. The flip flops are connected to wiring and are arranged to test connections in the wiring. The entire IP On Super-Sub (IPOS) device or each chip IP may be arranged to facilitate a scan test, a built-in self-test (BIST), etc., on the internal circuit of the chip IP.